LISTING OF THE CLAIMS

1-79. (Cancelled).

80. (Currently Amended) A method of operating an ~~active pixel CMOS~~ imager, comprising:

~~activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of~~ providing a first row select line and a shared column line for a first pixel of an array, and ~~said second address circuit consisting of~~ providing a second row select line and said shared column line for a second pixel of said array adjacent said first pixel, wherein said first pixel and said second pixel are in a row of pixels and do not share a row select line and the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array;

activating at least one of the first row select line and the second row select line~~, wherein the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array~~ to connect the associated one of the first and second pixels with the shared column line; and

~~generating an~~ outputting a signal over the shared column line ~~corresponding to charge accumulated~~ which is associated with the activated row select line by connecting at least one of the first pixel and second pixel to said shared column line.

81. (Currently Amended) The method of claim 80, wherein the shared column line ~~extends approximately linearly across the pixel array~~ connects with said first pixel and said second pixel at an S-shaped active area shared between the pixels.

82-83. (Cancelled).

84. (Currently Amended) A method of operating ~~a system~~ an imager, comprising:

~~focusing~~ receiving an image on ~~an active pixel CMOS imager, the imager comprising~~ a ~~pixel array;~~ pixel array comprising a

~~activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said~~ first pixel and ~~said~~ an adjacent second pixel ~~being~~ in a row of pixels, ~~said first address circuit consisting of~~ a first row select line and a shared column line provided for the first pixel, and ~~said second address circuit consisting of~~ a second row select line and said shared column line provided for the second pixel, each of said first and second pixels having a node for receiving photogenerated charges and a circuit for providing an output signal based on charges at said node to said shared column line in response to an associated activated row select line;

~~addressing the first pixel using the first row select line and then subsequently addressing the second pixel using the second row select line, the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row;~~

resetting a voltage level of [[a]] said node associated with the first pixel to a predetermined voltage using a reset transistor ~~addressed by a reset line that extends approximately linearly across the pixel array~~; and

~~transferring charge collected by~~ activating the first row select line to output a signal from the first pixel to the ~~node~~ shared column line [[;]]

~~detecting the charge at the node; and~~

~~generating an output signal over the shared column line, the output signal corresponding to the image~~.

85. (Currently Amended) The method of claim 84, wherein the shared column line ~~extends approximately linearly across the pixel array~~ connects with said first pixel and said second pixel at an S-shaped active area shared between the pixels.

86-87. (Cancelled).

88. (Currently Amended) An ~~active pixel CMOS~~ imager, comprising:

a plurality of pixels ~~to generate an output signal~~ for generating charge associated with detected light, the plurality of pixels arranged in rows and columns of an array, each said row having ~~both~~ interspersed odd and even pixels, wherein ~~each said~~ an odd pixel [[is]] of a row is addressed by ~~a respective first address circuit consisting essentially of~~ an activated odd row select line ~~and~~ to provide an output signal on a ~~shared~~ column line shared with an adjacent even pixel, and wherein ~~each said~~ the adjacent even pixel [[is]] of the row is addressed by ~~a respective second address circuit consisting essentially of~~ an activated even row select line ~~and a~~ to provide an output signal on the shared column line, wherein the even row select line[[s]] does not address the odd pixels and the odd row select line[[s]] does not address the even pixels;

~~a plurality of column lines comprising the column lines of the first address circuit and the second address circuit, each of the plurality of column lines being connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal;~~

a column driver to ~~address~~ access pixels connected to the shared column line[[s]]; and

a row driver to ~~address pixels through~~ selectively activate the odd row select line[[s]] and the even row select line[[s]].

89. (Currently Amended) The imager of claim 88, wherein the column lines ~~extend approximately linearly across the array~~ connects with said odd pixel and said even pixel at a respective S-shaped active area shared between the odd and even pixels.

90-92. (Cancelled).

93. (Currently Amended) A method of operating ~~a CMOS~~ an imager, comprising:

providing a first ~~address circuit~~ row select line exclusively for ~~even~~ first pixels of a row of pixels and a second ~~address circuit~~ row select line exclusively for ~~odd~~ second pixels of the row of pixels, ~~said first address circuit consisting essentially of an even row select line and~~ wherein said first and second row select lines connect said first and second pixels to respective ones of a plurality of shared column lines, which are each shared by adjacent first and second pixels, when the first and second row select lines are respectively activated, ~~and said second address circuit consisting essentially of an odd row select line and said plurality of shared column lines,~~ wherein the ~~even~~ first row select lines do not address ~~the odd~~ any second pixel[[s]] and the ~~odd~~ second row select lines do not address ~~the even~~ any first pixel[[s]];

addressing the ~~even~~ first pixels using a row driver coupled to the ~~even~~ first row select line;

providing a first output signal associated with light detected by the ~~even~~ first pixels to the respective ones of the plurality of shared column lines by activating the first row select line;

addressing the ~~odd~~ second pixels using the row driver coupled to the ~~odd~~ second row select line; and

providing a second output signal associated with light detected by the ~~odd~~ second pixels to the respective ones of the plurality of shared column lines by activating the second row select line.

94. (Currently Amended) The method of claim 93, wherein the shared column lines ~~extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line~~ connect with respective pairs of said first pixels and said second pixels at respective S-shaped active areas shared between the respective pairs of first and second pixels.

95-96. (Cancelled).

97. (Currently Amended) An ~~imaging device~~ imager, comprising:

a row comprising a first pixel and a second pixel;

the first and second pixels being joined by a ~~diagonal~~ common active area component;

~~a first even row line connected with the first pixel;~~

~~a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row;~~

a column line connected with the first and second pixels at the ~~diagonal~~ common active area component, wherein said common active area component is diagonal where it connects the first pixel and the second pixel with respect to the column line;

a first ~~address circuit for the first pixel consisting essentially of the first even~~ row select line ~~and a shared~~ for connecting the first pixel with the column line to allow an output signal to be transferred from the first pixel to the column line; and

a second ~~address circuit for the second pixel consisting essentially of the second odd~~ row select line ~~and a shared~~ for connecting the second pixel with the column line to allow an output signal to be transferred from the second pixel to the column line, wherein the first row select line does not address the second pixel and the second row select line does not address the first pixel.

98. (Currently Amended) The ~~imaging device~~ imager of claim 97, wherein the row further comprises a plurality of first pixels and a plurality of second pixels.

99. (Currently Amended) The ~~imaging device~~ imager of claim 97, wherein the ~~first even row line and second odd row line each extends substantially linearly across an array of pixels~~ common active area component and the first and second pixels are laid out in an S-shape.

100-101. (Cancelled).

102. (Currently Amended) An ~~imaging device~~ imager, comprising:

a pixel array comprising a row of first pixels and second pixels;

a first ~~address~~ circuit for the first pixels ~~consisting essentially of~~ comprising a first row select line ~~and~~ for connecting the first pixels with respective ones of a plurality of shared column lines; and

a second ~~address~~ circuit for the second pixels ~~consisting essentially of~~ comprising a second row select line ~~and~~ for connecting the second pixels with said respective ones of said plurality of shared column lines, wherein the first row select lines do not address the second pixels and the second row select lines do not address the first pixels, each of the shared column lines being associated with a first pixel and a second pixel~~; and~~

~~a reset line connected to the first pixels~~.

103. (Currently Amended) The ~~imaging device~~ imager of claim 102, wherein the plurality of first pixels are every other pixel in the row.

104. (Currently Amended) The ~~imaging device~~ imager of claim 102, wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line.

105. (Currently Amended) The ~~imaging device~~ imager of claim 102, wherein each pair of first and second pixels are connected by a substantially diagonal active area such that the paired pixels are laid out in an S-shape.

106. (Currently Amended) An ~~imaging device~~ imager comprising:

a row of pixels comprising a first plurality of pixels and a second plurality of pixels;

a first address circuit for the first plurality of said pixels and a second address circuit for the second plurality of said pixels, said first address circuit ~~consisting essentially of~~ comprising a first row select line and a plurality of shared column lines, and said second address circuit ~~consisting essentially of~~ comprising a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second plurality of pixels and the second row select lines do not address the first plurality of pixels, each of said plurality of shared column lines being connected to a respective first pixel of the first plurality of pixels and a respective second pixel of the second plurality of pixels by the first row select line and the second row select line; and

a reset line connected to at least the first plurality of pixels or the second plurality of pixels.

107. (New) A pixel array, comprising:

a row of a plurality of first pixels alternated with a plurality of second pixels;

a first row select line dedicated to only said row and only the first pixels of said row, wherein said first row select line controls a signal output switch for a plurality of first pixels of said row;

a second row select line dedicated to only said row and only the second pixels of said row, wherein said second row select line controls a signal output switch for a plurality of second pixels of said row; and

at least one common output line shared by said row and a plurality of other rows of pixels, wherein said common output line is shared by at least a pair of adjacent first and second pixels of said row.

108. (New) The pixel array of claim 107, wherein the common output line connects with said pair of adjacent first and second pixels at an S-shaped active area shared between the at least one first and second pixels.

109. (New) A pixel array, comprising:

a row of pixels, including odd column pixels alternated with even column pixels;

an odd output selection circuit for connecting an odd column pixel of the row to a column output line, the odd output selection circuit being driven by an odd pixel selection signal line common to only the odd column pixels of the row; and

an even output selection circuit for connecting an even column pixel of the row to the column output line, the even output selection circuit being driven by an even pixel selection signal line common to only the even column pixels of the row.

110. (New) The pixel array of claim 109, wherein the column output line connects with the odd column pixel and the even column pixel at an S-shaped active area shared between the odd and even column pixels.

111. (New) A pixel array, comprising:

a first pixel comprising a first photodiode, a first source follower transistor configured to provide a pixel output signal based on charges collected by the first photodiode, and a first pixel output selection switch configured to connect the output signal of the first source follower transistor to an output line; and

a second pixel adjacent the first pixel comprising a second photodiode, a second source follower transistor configured to provide a pixel output signal based on charges collected by the second photodiode, and a second pixel output selection switch configured to connect the output signal of the second source follower transistor to the output line, wherein the output line is shared between the first pixel and the second pixel.

112. (New) The pixel array of claim 111, wherein the output line connects with the first pixel and the second pixel at an S-shaped active area shared between the first and second photodiodes.

113. (New) An imager structure, comprising:

a pixel array having pixels arranged in rows and columns;

said pixel array comprising a first pixel and a second pixel formed in respectively adjacent columns and in conjunction with an active area spanning between a first photodetector of the first pixel and a second photodetector of the second pixel but no other photodetectors, said active area having the first associated photodetector and the second associated photodetector at opposite ends of said active area; and

a common output for charges generated from the first photodetector and the second photodetector at a portion of said active area between said first and second photodetectors, the common output being coupled to a column line shared by the first pixel and the second pixel, wherein the portion of said active area to which the common output is connected is configured diagonally with respect to an extending direction of said column line within the pixel array.

114. (New) The pixel array of claim 113, wherein the active area shared between the first and second pixels is S-shaped.

115. (New) A pixel array, comprising:

a first pixel and a second pixel, the first pixel having a first photodetector and the second pixel having a second photodetector, wherein the first photodetector shares an active area with the second photodetector and no other photodetector, said shared active area providing an output for said first and second photodetectors; and

a common readout line for receiving a signal from said first and second photodetectors the active area shared by the first pixel and the second pixel, wherein the shared active area is oriented diagonally relative to an extending direction of the common readout line across the pixel array.

116. (New) The pixel array of claim 115, wherein the active area shared by the first and second pixels is S-shaped.

117. (New) A pixel array, comprising:

a first pixel and a second pixel, said first pixel having a first photodetector and said second pixel having a second photodetector, wherein said first photodetector shares an active area with said second photodetector and no other photodetector and at least one of said first pixel and said second pixel further comprises a reset transistor, said reset transistor comprising a gate, a first source/drain region, and a second source drain region linearly arranged, wherein said shared active area between the first and second photodetectors has a diagonal orientation relative to the linear arrangement of the reset transistor; and

a common readout line for receiving charge from said shared active area.